Amendments to the Claims

Please amend the claims in the manner indicated.

1. (currently amended) An apparatus, comprising:

a first circuitry to permit access, responsive to entering a first password, to a first set of resources to debug a first set of code in a memory;

a storage structure to contain a second password; [[and]]

a second circuitry coupled to the first circuitry and to the storage structure to permit access, responsive to entering the second password, to a second set of resources to debug a second set of code in the memory; and

circuitry to prevent the access responsive to said entering the first password if the access responsive to said entering the second password is enabled, and to prevent the access responsive to said entering the second password if the access responsive to said entering the first password is enabled.

2. (original) The apparatus of claim 1, wherein said access to the second set of resources is through a debug interface.

3. (original) The apparatus of claim 2, adapted to place the second set of code in a substantially different portion of the memory than the first set of code.

4. (original) The apparatus of claim 1, wherein the storage structure comprises a content addressable memory.

5. (cancelled)

6. (original) The apparatus of claim 1, wherein the storage structure comprises a programmable storage structure.

7. (original) The apparatus of claim 1, wherein said first set of resources comprises a first portion of the memory and said second set of resources comprises a second portion of the memory different than the first portion.

8. (original) The apparatus of claim 1, wherein the second set of resources is substantially a subset of the first set of resources.

9. (original) A system, comprising:

a volatile first memory;

a second memory coupled to the first memory to contain code for execution;

a processor coupled to the second memory to execute the code;

a first storage structure coupled to the processor to contain a first password;

a second storage structure coupled to the processor to contain a second password; and

circuitry to permit access, responsive to entering the first password, to a first set of resources to debug a first set of code in the second memory, to disable said access to the first set of resources, and to enable access, responsive to entering the second password, to a second set of resources to debug a second set of code in the second memory.

10. (original) The system of claim 9, wherein the first and second access are to be through a debug interface.

11. (original) The system of claim 9, wherein the second storage structure is a content addressable memory.

12. (original) The system of claim 9, wherein the circuitry is adapted to cause the access responsive to said entering the first password and the access responsive to said entering the second password to be mutually exclusive.

13. (original) A method, comprising:

disabling a first password that enables performing a first set of code debug operations;

storing a second password; and

entering the second password to enable performing a second set of code debug operations;

wherein being enabled to perform the first set of code debug operations and being enabled to perform the second set of code debug operations are mutually exclusive.

14. (original) The method of claim 13, wherein said being enabled to perform the second set of code debug operations comprises being enabled to perform a subset of the first code debug operations.

15. (original) The method of claim 13, wherein said first and second code debug operations are performed through a debug interface.

16. (original) The method of claim 13, wherein said disabling the first password results from said storing the second password.

17. (original) The method of claim 13, further comprising enabling a third password that re-enables said performing the first set of code debug operations.

18. (currently amended) A tangible machine-readable medium that provides instructions, which when executed by a computing platform, cause said computing platform to perform operations comprising:

receiving a first password to enable debug of a first set of code during a first debug stage;

disabling the first password to prevent further debugging activities during the first debug stage;

storing a second password; and

receiving the second password to enable debug of a second set of code during a second debug stage;

wherein the operation of disabling the first password prevents access to the first set of code during the second debug stage.

19. (cancelled)

20. (original) The medium of claim 18, wherein the operation of storing the second password results in said disabling the first password.

21. (original) The medium of claim 18, wherein said operations further comprise using a third password to re-enable the debug of the first set of code.

22-35. (cancelled)